PRINTER RUSH
(PTO ASSISTANCE)

Application :	10/604509	**Examiner :**	Nang	**GAU :**	2818
From:	J. Black	**Location:**	(IDC) FMF FDC	**Date:**	5/17/05

Tracking #: 06092155 Week Date: 4/4/05

DOC CODE	DOC DATE	MISCELLANEOUS
☐ 1449		☐ Continuing Data
☐ IDS		☐ Foreign Priority
☒ CLM	2/18/05	☐ Document Legibility
☐ IIFW		☐ Fees
☐ SRFW		☐ Other
☐ DRW		
☐ OATH		
☐ 312		
☒ SPEC	2/18/05	

[RUSH] **MESSAGE:** Please provide a more legible copy of SPEC dated 2/18/05 and CLM dated 2/18/05.

Thank you!

[XRUSH] **RESPONSE:** ~~See attached letter~~

Corrected

Belinda Lee **INITIALS:** BS

NOTE: This form will be included as part of the official USPTO record, with the Response document coded as XRUSH.

REV 10/04

bclinda@xipgroup.com TW 5/20 5/24

10380-US.PA

Patent 10/604,509

Customer No.: 31561
Docket No.10380-US-PA
Application No.: 10/604,509

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	
Applicant	: Yeh et al.
Application No.	: 10/604,509
Filed	: 2003/7/28
For	: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
Art Unit	: 2818
Examiner	: DANG, PHUC T

TRANSMITTAL LETTER
002-1-703-746-4272
(Via fax: 1+ 15 pages)

Ms. Patricia Small
U. S. Patent and Trademark Office
Alexandria, VA 22314

Dear Ms. Small,

Per the request made in your e-mail of May 25, 2005, transmitted herewith is a copy of the response filed with the Office on February 18, 2005.

Thank you for your attention to the subject matter. If you need further information, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: June 1, 2005 By: Belinda Lee
Belinda Lee
Registration No.: 46,863

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Patent

Customer No.: 31561
Docket No.10380-US-PA
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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For	: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF
Art Unit	: 2818
Examiner	: DANG, PHUC T

TRANSMITTAL LETTER
002-1-703-872-9306
(Via fax: 1+ 14 pages)

Assistant Commissioner for Patents
Arlington, Virginia 22202

Dear Sir,

In response to the Office Action dated November 19, 2004(Paper No.: 1104), please find the *Response to Non-Final Office Action*, in14 pages.

I believe that no fee is incurred. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.:10380 -US-PA)

Thank you for your assistance in the subject matter. If you have any questions, please feel free to contact me.

Respectfully Submitted,
JIANQ CHYUN Intellectual Property Office

Date: February 18, 2005 By: Belinda Lee
Belinda Lee
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Customer No.: 31561
Application No.: 10/604,509
Docket No.: 10380-US-PA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Examiner: Dang, Phuc T.

Group Art Unit: 2818

In re PATENT APPLICATION of
Applicants : Fang-Yu Yeh

Serial No. : 10/604,509

Filed : July 28, 2003

For : Semiconductor Device And Manufacturing Method Thereof

AMENDMENT

Attorney Docket: 10380-US-PA

No fee is believed to be due. However, the Commissioner is authorized to charge any fees required in connection with the filing of this paper to account No. 50-2620 (Order No.:10380-US-PA)

RESPONSE TO NON-FINAL OFFICE ACTION

U.S. Patent and Trademark Office
Commissioner for Patents
220 20th Street South
Customer Window, Mail Stop Amendment
Crystal Plaza Two, Lobby, Room 1B03
Arlington, Virginia 22202

Sir:

In response to the Office Action dated November 19, 2004, please enter the following amendments and consider the following remarks.

AMENDMENTS TO SPECIFICATION

Please amend the specification as follows.

[0012] An object of this invention is to provide a semiconductor device and manufacturing method thereof having a lower overall thermal budget.

[0013] An object of this invention is to provide a semiconductor device and manufacturing method thereof capable of producing an internal structure with a lower aspect ratio so that the process window for etching out contacts is increased.

[0014] An object of this invention is to provide a semiconductor device and manufacturing method thereof capable of producing a device with optimal short channel properties.

AMENDMENTS TO CLAIMS

Please amend claims as follows.

1. (currently amended) A method of manufacturing a semiconductor device, comprising the steps of:

providing a substrate;

forming a mask layer over the substrate;

patterning the mask layer and the substrate to form a first opening in the substrate;

forming a gate dielectric layer~~, a first conductive layer~~ and a polycide ~~second conductive~~ layer inside the first opening sequentially, wherein the ~~gate dielectric layer covers the interior surface of the first opening, the first conductive layer covers the gate dielectric layer and the second conductive~~ polycide layer ~~completely~~ fills the first opening;

removing a portion of the ~~first conductive layer and the second conductive~~ polycide layer so that ~~the~~ an upper surface of a ~~remaining first conductive layer and a remaining second conductive~~ remainder polycide layer in the first opening ~~are~~ is at a level slightly below ~~the~~ an upper surface of the substrate and thereby form a second opening;

forming a cap layer inside the second opening;

removing the mask layer; and

forming a source/drain region in the substrate.

2. (original) The method of claim 1, wherein the step of forming the source/drain region is performed after the step of removing the mask layer.

3. (original) The method of claim 1, wherein the step of forming the source/drain region in the substrate is performed before the step of forming the mask layer over the substrate.

4. (original) The method of claim 3, further comprises a step of forming a well region in the substrate before the step of forming source/drain region in the substrate.

5. (original) The method of claim 4, wherein the step of forming the source/drain region and the step of forming the well region in the substrate use the same layer as a implanting mask.

6. (original) The method of claim 1, further comprises a step of forming a well region in the substrate before the step of forming the mask layer on the substrate.

7. (original) The method of claim 1, wherein after the step of forming a mask layer over the substrate, furthermore comprises forming a bottom anti-reflection layer over the mask layer; and the step of patterning the mask layer and the substrate to form a first opening furthermore comprises patterning the bottom anti-reflection layer.

Claim 8 (canceled).

9. (currently amended) The method of claim 1, wherein the polycide ~~second conductive~~ layer comprises a polysilicon layer and a refractory metal silicide layer.

10. (currently amended) The method of claim 9, wherein a material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide,

nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

11. (currently amended) The method of claim 1, wherein the step of removing a portion of the ~~first conductive layer and the second conductive~~ polycide layer comprises:

performing a chemical-mechanical polishing process to remove a portion ~~portions of the first conductive layer and the second conductive~~ polycide layer outside the first opening; and

etching back the remainder polycide ~~first conductive layer and the second conductive~~ layer in the first opening ~~so that the~~ until an upper surface of ~~the~~ a remaining polycide ~~first conductive layer and the remaining second conductive~~ layer in the first opening are at a level slightly below the upper surface of the substrate and thereby form a second opening.

12. (original) The method of claim 1, wherein the mask layer is fabricated using a material having an etching selectivity that differs from the material constituting the first conductive layer, the second conductive layer and the cap layer.

13. (currently amended) The method of claim 1, wherein after the step of patterning the mask layer and the substrate to form the first opening further comprises performing a threshold voltage adjustment process.

14. (original) The method of claim 1, further comprising:

forming an inter-layer dielectric layer over the substrate; and

forming a contact opening in the inter-layer dielectric layer using the cap layer as a self-aligned mask.

Claims 15-23 (canceled).

24. (new) A method of manufacturing a semiconductor device, comprising the steps of:

forming an opening in a substrate;

forming a doped polysilicon layer over the sidewalls of the opening; and

forming a polycide layer over the doped polysilicon layer inside the opening such that an upper surface of the polycide layer is lower than a top surface of the substrate, wherein sidewalls of the polycide layer is enclosed by the doped polysilicon layer.

25. (new) The method of claim 24, wherein the polycide layer comprises a polysilicon layer and a refractory metal silicide layer.

26. (new) The method of claim 25, wherein a material constituting the refractory metal silicide layer is selected from a group consisting of tungsten silicide, nickel silicide, cobalt silicide, titanium silicide, molybdenum silicide, platinum silicide and palladium silicide.

27. (new) The method of claim 1, wherein the step of forming the polycide layer comprises:

sequentially forming a polysilicon layer and a refractory metal silicide layer over the doped polysilicon layer and filling the opening;

performing a chemical-mechanical polishing process to remove portions of the polysilicon layer and the refractory metal silicide layer outside the opening; and

etching back the remainder portions of the polysilicon layer and the refractory metal silicide layer in the opening until an upper surface of a remaining portions the polysilicon layer and the refractory metal silicide layer in the opening layer in the opening are at a level below the upper surface of the substrate.

REMARKS

Present Status of the Application

It is noted with great appreciation that the Examiner deems claims 13-14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claim.

Claims 1-27 are pending of which claims 1, 9-10 and 13 have been amended, claim(s) 8 (and 15-23) has been canceled without prejudice and disclaimer, and claims 24-27 have been newly added, to more explicitly describe the claimed invention. Furthermore, the specification has been amended to correct some minor typographical errors. It is believed that no new matter adds by way of amendments to claims, specification or otherwise to the application. For at least the following reasons, Applicants respectfully submit that claims 1-14 and 24-27 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of the claim rejection under 35 USC 103

1. The Office Action rejected claims 1-6, 8 and 11-12 under 35 USC 103(a) as being unpatentable over Tseng et al. (US-5,677228, hereinafter Tseng) and further in view of Nam et al. (US-6,765,252, hereinafter Nam).

In rejecting the above claims, the Examiner stated that Tseng discloses all the features of the claimed invention except for the steps of forming a cap layer inside the second opening; removing the mask layer; and forming a source/drain region in the

substrate. However, the Examiner relied upon Nam to disclose these steps, wherein Nam shows a step of forming a cap layer (45, FIG. 8) inside the second opening; removing the mask layer (46, FIG. 8); and forming a source/drain region (41, FIG. 9) in the substrate. It would have been obvious to one skilled in the art at the time of the invention to apply the teaching of Nam to Tseng discussed above such that a step of forming a cap layer inside the second opening, removing the mask layer and forming a source/drain region in the substrate for a purpose of improving a manufacturing of a semiconductor device.

Applicants respectfully disagree and traverse the above rejections of the Examiner as follows. Applicants respectfully submit that the independent claim 1, as amended, is allowable for at least the reason that both Tseng and Nam fail to teach, suggest or disclose every features of the amended proposed independent claim 1. More specifically, both Tseng and Nam fail to teach, suggest or disclose a method of fabricating a semiconductor device comprising at least "forming a gate dielectric layer and a polycide layer inside the first opening sequentially, wherein the polycide layer fills the first opening" as required by the amended proposed independent claim 1. The advantage of the above process step is that because the polycide layer is formed inside the opening, therefore the sidewalls of the polycide layer is not directly exposed to the subsequent thermal oxidation process. Thus, lateral growth of the polycide layer can be effectively reduced.

Applicants respectfully submit that the presents inventors recognized that when the polycide layer comprising, for example, a polysilicon layer and the tungsten silicide

layer, is NOT formed inside an opening, the sidewalls sidewalls of the polycide layer are directly exposed to the thermal oxidation process, consequently, the tungsten silicide layer may react with the oxygen to form tungsten oxide and therefore lateral extrusions (as shown in Figure 1D) are often formed on the sidewalls of the tungsten silicide layer and may undesirable electrically connect with neighboring conductive structures causing short circuits and thereby adversely affect the performance of the semiconductor device. In order to remedy the above problems, the present inventors proposed forming the polycide layer inside the opening of the substrate so that the sidewalls of the polycide layer is not directly exposed to the thermal oxidation and also the sidewalls of the polycide layer is supported by the sidewalls of the opening. Thus, the lateral extrusions from the sidewalls of the polycide layer can be effectively reduced.

Instead, Tseng, Fig. 5, lines 5-15 of col. 3, substantially teaches a process of forming a resistor comprising the steps of forming an undoped polysilicon layer (44) over the oxide layer (42) and a heavily-doped polysilicon layer (46) over the undoped polysilicon layer (44) inside the trench (40). Therefore, it is clear that Tseng substantially fails to teach, suggest or hint forming a polycide layer inside the opening as required by the proposed amended claim 1, instead Tseng substantially teaches forming a polysilicon resistor (44, 46) inside the trench (40).

Furthermore, because Tseng substantially teaches a process of forming a polysilicon resistor (44, 46) inside the trench, therefore, Tseng cannot possibly recognize the problems associated with polycide gate structure during the thermal oxidation much less teachings on remedy of the problems due to formation of lateral

extrusions from the sidewalls of the polycide layer, which the present inventors propose to resolve. Therefore, it is clear that Tseng cannot possibly suggest one skilled in the art to form a polycide layer inside the opening of the substrate for remedying the problems caused by the exposure of the sidewalls of the polycide layer to the thermal oxidation process as proposed by the present inventors.

Furthermore, because Nam also fails to teach, suggest or disclose a process of forming a polycide layer within the opening/trench, and therefore, Nam cannot possibly cure the specific deficiencies of Tseng for at least the reasons substantially discussed above. Accordingly, Applicants respectfully submit that both Tseng and Nam, neither alone nor in combination, render every features of the amended proposed Claim 1 obvious in this regard.

Because, the newly added proposed independent claim 24 also recite features similar to those recited by the amended proposed claim 1, therefore, Applicants similarly submit that the new proposed independent claim 24 also patently define over Tseng and Nam for at least the same reasons discussed above.

Furthermore, the new independent claim 24 further recites "forming the polycide layer over the doped polysilicon layer inside the opening, wherein the sidewalls of the polycide layer is enclosed by the doped polysilicon layer". The advantage of the above feature is that at least the thermal oxidation of the polycide layer can be effectively reduced by the doped polysilicon layer. Applicants respectfully submit that both Tseng and Nam substantially fail teach, suggest or hint at least a step of forming the polycide layer over the doped polysilicon layer inside the opening, wherein the sidewalls of the

polycide layer is enclosed by the doped polysilicon layer, instead, Tseng substantially teaches forming a polysilicon resistor (44, 46) over the oxide layer (42), wherein the sidewalls of the polysilicon resistor (44, 46) is enclosed by the oxide layer (42); and Nam fails to even mention forming a polycide layer inside an opening. Thus, Applicants respectfully submit that both Tseng and Nam substantially fail to teach, suggest or hint the above feature of the new claim 24 as well.

Claims 2-6, 11-12 and 24-27, which directly or indirectly depend from claims 1 and 24 respectively, are also patentable over Tseng and Nam at least because of their dependency from an allowable base claim.

For at least the above reasons, it is therefore submitted that claims 1-6, 11-12 and 24-27 patently define over Tseng and Nam and therefore claims 1-6, 11-12 and 24-27 should be allowed. Reconsideration and withdrawal of these rejections is respectfully requested.

2. *The Office Action rejected claim 7 under 35 USC 103(a) as being unpatentable over Tseng and Nam in view of Liu et al. (US-6,509,249, hereinafter Liu).*

Applicants respectfully disagree and would like to point out that even though the Examiner relied upon Liu to disclose the mask layer and the anti-reflection layer, still Liu cannot cure the specific deficiencies of Tseng and Nam for at least the same reasons discussed above. Therefore, claim 7 also patently define over Tseng, Nam and Liu for at least the same reasons discussed above. Reconsideration and withdrawal of the above rejections is respectfully requested.

3. The Office Action rejected claims 9-10 under 35 USC 103(a) as being unpatentable over Tseng and Nam in view of Liu et al. (US-6,046,108, hereinafter Liu'108).

Applicants respectfully disagree and would like to point out that even though the Examiner relied upon Liu'108 to disclose the materials of refractory metal silicide layer, still Liu'108 cannot cure the specific deficiencies of Tseng and Nam for at least the same reasons discussed above. Therefore, claims 9-10 also patently define over Tseng, Nam and Liu'108 for at least the same reasons discussed above. Reconsideration and withdrawal of the above rejections is respectfully requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-14 and 24-27 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted

Date : February 28, 2005

Belinda Lee
Registration No.: 46,863

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